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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/26/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	09/977,089	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-27,29-32 and 40-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-27,29-32 and 40-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08). Paper No(s)/Mail Date *20060602*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-7, 9-14, 16-17, 20-24, and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" ("MCF5206") and Freescale Semiconductor, Inc. "Addendum to MCF5206 User Manual" ("MCF5206 Addendum"), and US Patent Number 5,025,368 to Watanabe ("Watanabe") and US Patent Number 6,499,078 to Beckert et al. ("Beckert").

3. In reference to Claim 1, MCF5206 discloses a plurality of first interrupts generated by devices internal to the microprocessor, said plurality of first interrupts having programmable priorities (See 'Interrupt Controller' on Page 5); a plurality of second interrupts that are generated external to the core, said second interrupts having architecturally fixed priorities (See 'Interrupt Controller' on Page 5). MCF5206 will inherently have a priority encoder coupled to the first and second interrupts and a vector

generator for prioritizing the interrupts utilizing programmable priorities for the first interrupts and fixed priorities for the second interrupts (See Page 2 'System Interface' – 'Programmable Interrupt Controller'). MCF5206 further discloses storing a programmable interrupt value for the internal interrupts (See "'Interrupt Controller' on Page 5) and a vector generator (See Page 2 'System Interface' – 'Programmable Interrupt Controller') but is silent as to the structure. Beckert teaches an interrupt controller having interrupts with programmable priorities, having a status register (See Figure 2 Number 40), said status register comprising a vector table (See Figure 2 Number 50), and an interrupt register, said interrupt register coupled to said vector table, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities (See Figure 2 Number 48 and Column 3 Line 61 – Column 4 Line 42). MCF5206 does not disclose that the first interrupts are generated by the core. Watanabe teaches a CPU core comprising segments commonly used to form a complete microprocessor, such as timers and I/O units (See Column 1 Lines 55-57 and Column 2 Lines 50-55), as well as additional function blocks (See Column 3 Lines 28-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206 with priority value storage means and vector table storage means of Beckert and with the internal peripheral devices as part of the core, resulting in the invention of Claim 1, because MCF5206 is silent as to the structure of how it stores the interrupt priority values and vector table, and one would naturally look to interrupt systems having programmable priorities when

constructing the device, and because the priority registers and address registers provide an easy means for changing the priority levels and servicing information for any given interrupt source (See Column 2 Lines 11-22 of Beckert); and to allow it to be easily interfaced with various different peripheral devices, to minimize the area needed by the microprocessor by reducing the area needed for connecting lines, and to provide greater flexibility in program design (See Column 1 Lines 42-45; Column 3 Lines 41-46; and Column 4 Lines 1-16 of Watanabe).

4. In reference to Claim 2, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 1 above. MCF5206 further discloses that the plurality of first interrupts comprise timer interrupts, which are hardware interrupts (See 'Timer Module' on Page 4). MCF5206 Addendum discloses that the MCF5206 also includes a TRAP instruction, which is a software interrupt (See Page 5).

5. In reference to Claim 4, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 1 above. MCF5206 further discloses that the core executes instructions (See Page 1 Paragraph 3).

6. In reference to Claim 5, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 1 above. MCF5206 further discloses providing the plurality of second interrupts to the priority controller with predefined interrupt priorities (See 'Interrupt Controller' on Page 5).

7. In reference to Claim 6, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 1 above. The priority encoder of MCF5206 will inherently produce an indication of which of the first and second plurality of interrupts has the highest priority.

8. In reference to Claim 7, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 6 above. MCF5206 further discloses a vector generator for producing an interrupt vector corresponding to the interrupt having the highest priority (See Page 2 'System Interface' – 'Programmable Interrupt Controller').

9. In reference to Claim 9, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 1 above. Beckert further teaches that the configurable priority registers are writable by the processing system (See Column 3 Lines 1-9).

10. In reference to Claim 10, MCF5206 discloses a microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller, the first interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5), the microprocessor comprising: a core for executing instructions (See Page 1 Paragraph 3); and generating second interrupts by devices internal to the microprocessor (See 'Interrupt Controller' on Page 5). Because the interrupt priorities are programmable, MCF5206 must the programmable priorities of the second interrupts

(See 'Interrupt Controller' on Page 5), but is silent as to the structure. Beckert teaches an interrupt controller having interrupts with programmable priorities and an interrupt register having a plurality of configurable priority registers for storing said programmable priorities (See Figure 2 Number 48 and Column 3 Line 61 – Column 4 Line 42). MCF5206 will inherently have a priority encoder coupled to the core for prioritizing the first and second interrupts utilizing the fixed priorities for the first interrupts and the programmable priorities for the second interrupts (See Page 2 'System Interface' – 'Programmable Interrupt Controller'). MCF5206 does not disclose that the second interrupts are generated by the core. Watanabe teaches a CPU core comprising segments commonly used to form a complete microprocessor, such as timers and I/O units (See Column 1 Lines 55-57 and Column 2 Lines 50-55), as well as additional function blocks (See Column 3 Lines 28-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206 with priority value storage means and vector table storage means of Beckert and with the internal peripheral devices as part of the core, resulting in the invention of Claim 10, because MCF5206 is silent as to the structure of how it stores the interrupt priority values and vector table, and one would naturally look to interrupt systems having programmable priorities when constructing the device, and because the priority registers and address registers provide an easy means for changing the priority levels and servicing information for any given interrupt source (See Column 2 Lines 11-22 of Beckert); and to allow it to be easily interfaced with various different peripheral devices, to minimize the area needed

by the microprocessor by reducing the area needed for connecting lines, and to provide greater flexibility in program design (See Column 1 Lines 42-45; Column 3 Lines 41-46; and Column 4 Lines 1-16 of Watanabe).

11. In reference to Claim 11, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206 further discloses that the interrupt controller receives a plurality of third interrupts from sources thereof, prioritizes said third interrupts, and provides the prioritized third interrupts to the microprocessor as the first interrupts (See 'Interrupt Controller' on Page 5).

12. In reference to Claim 12, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 11 above. MCF5206 further discloses that the first interrupts are presented to the processor on first interrupt signal lines attached to the microprocessor (See Figure on Page 6).

13. In reference to Claim 13, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206 Addendum discloses that the instructions executed by the core of the MCF5206 comprise: JSR, BSR, and RTS instructions, which are both instructions for handling the first interrupts and instructions for handling the second interrupts (See Pages 3-5). MCF5206 further discloses third instructions for storing said programmable priorities into said priority storage means (See 'Interrupt Controller' on Page 5).

14. In reference to Claim 14, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206 further discloses that the plurality of first interrupts comprise timer interrupts, which are hardware interrupts (See 'Timer Module' on Page 4). MCF5206 Addendum discloses that the MCF5206 also includes a TRAP instruction, which is a software interrupt (See Page 5).

15. In reference to Claim 16, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. Beckert further teaches that the priority storage logic includes a plurality of interrupt fields each corresponding to one of the interrupts (See Figure 2 and Column 3 Line 61 – Column 4 Line 42).

16. In reference to Claim 17, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 16 above. MCF5206 further discloses that each internal interrupt signal can be programmed to one of 7 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 28 distinct interrupt priorities which require a minimum 5-bit field (which allows a maximum of 32 distinct values) to store. A 4-bit field is a subset of a 5-bit field, and thus a 4-bit field providing 16 distinct interrupt priorities is inherently a part of MCF5206.

17. In reference to Claim 20, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206 further discloses that each external

interrupt signal can be programmed to one of 3 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 12 distinct interrupt priorities. Eight distinct interrupt priorities is a subset of a 12 distinct interrupt priorities, and thus 8 distinct interrupt priorities for the first interrupts is inherently a part of MCF5206.

18. In reference to Claim 21, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 20 above. MCF5206 further discloses that each internal interrupt signal can be programmed to one of 7 interrupt levels each having 4 priority levels (See 'Interrupt Controller' on Page 5), thus providing 28 distinct interrupt priorities. The 28 internal interrupt levels overlap with the 12 external interrupt levels (See 'Interrupt Controller' on Page 5).

19. In reference to Claim 22, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206 further discloses that that the priority encoder, when prioritizing the first and second interrupts, also uses priorities for the first interrupts established by the interrupt controller (See 'Interrupt Controller' on Page 5).

20. In reference to Claim 23, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. The priority encoder of MCF5206 will

inherently produce an indication of which of the first and second plurality of interrupts has the highest priority.

21. In reference to Claim 24, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 23 above. MCF5206 further discloses a vector generator for producing an interrupt vector corresponding to the interrupt having the highest priority (See Page 2 'System Interface' – 'Programmable Interrupt Controller').

22. In reference to Claim 40, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 1 above. MCF5206 further discloses that the priority encoder is configured to merge said first interrupts and said second interrupts for purposes of determining priority (See 'Interrupt Controller' on Page 5).

23. In reference to Claim 41, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 40 above. MCF5206 further discloses that the first interrupts have architecturally fixed priorities and the second interrupts have values which are intermediate to the fixed priorities (See 'Interrupt Controller' on Page 5).

24. In reference to Claim 42, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206 further discloses that the priority encoder is configured to merge said first interrupts and said second interrupts for purposes of determining priority (See 'Interrupt Controller' on Page 5).

25. In reference to Claim 43, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 42 above. MCF5206 further discloses that the first interrupts have architecturally fixed priorities and the second interrupts have values which are intermediate to the fixed priorities (See 'Interrupt Controller' on Page 5).

26. Claims 27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Motorola MCF5206 Integrated Microprocessor, as described in MCF5206 and MCF5206 Addendum, and Watanabe.

27. In reference to Claim 27, MCF5206 discloses a method for prioritizing peripheral and external interrupts in a processing system, comprising: receiving the external interrupts, the external interrupts having architecturally fixed interrupt priorities (See 'Interrupt Controller' on Page 5); receiving the peripheral interrupts, the peripheral interrupts having programmable priority levels which are intermediate to the architecturally fixed interrupt priorities for the off-core interrupts (See 'Interrupt Controller' on Page 5). MCF5206 will inherently prioritize the on-core and off-core interrupts according to their priority levels and produce an indication of which of the first and second plurality of interrupts has the highest priority. MCF5206 does not disclose that the peripheral interrupts are generated by the core. Watanabe teaches a CPU core comprising segments commonly used to form a complete microprocessor, such as

timers and I/O units (See Column 1 Lines 55-57 and Column 2 Lines 50-55), as well as additional function blocks (See Column 3 Lines 28-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the MCF5206 with the internal peripheral devices as part of the core, resulting in the invention of Claim 10, in order to allow it to be easily interfaced with various peripheral devices, to minimize the area needed by the microprocessor by reducing the area needed for connecting lines, and to provide greater flexibility in program design (See Column 1 Lines 42-45; Column 3 Lines 41-46; and Column 4 Lines 1-16 of Watanabe).

28. In reference to Claim 29, MCF5206 and Watanabe disclose the limitations as applied to Claim 27 above. MCF5206 further discloses that the off-core interrupts are initially prioritized by an interrupt controller (See 'Interrupt Controller' on Page 5).

29. In reference to Claim 30, MCF5206 and Watanabe disclose the limitations as applied to Claim 27 above. MCF5206 will inherently select the received internal or off-core interrupt with the highest priority level by examining the priority levels of each of the received internal and off-core interrupts (See 'Interrupt Controller' on Page 5).

30. Claims 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the MCF5206, Watanabe, and Beckert as applied to Claim 2 above, and further in view of US Patent Number 5,768,500 to Agrawal et al. ("Agrawal").

31. In reference to Claim 3, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 2 above. MCF5206 further discloses that interrupts can be generated by hardware timers (See 'Timer Module' on Page 2). MCF5206, Watanabe, and Beckert do not disclose that said hardware interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206, Watanabe, and Beckert with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 3, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

32. In reference to Claim 15, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 14 above. MCF5206 further discloses that interrupts can be generated by hardware timers (See 'Timer Module' on Page 2). MCF5206, Watanabe, and Beckert do not disclose that said hardware interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206, Watanabe, and Beckert with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 15, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization architectures, operating systems, compilers, and applications (See Column 1 Line 50-Column 2 Line 6 of Agrawal).

33. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the MCF5206, Watanabe, and Beckert as applied to Claim 10 above, and further in view of US Patent Number 5,148,544 to Cutler et al. ("Cutler").

34. In reference to Claim 18, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 10 above. MCF5206, Watanabe, and Beckert do not disclose that said priority storage means is located within a privileged resource within the microprocessor. Cutler teaches that a register for storing information related to an interrupt condition is accessible only during a privileged mode (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206, Watanabe, and Beckert with the privileged mode register access of Cutler, resulting in the invention of Claim 18, in

order to prevent a compromise of the security of other users or programs (See Column 7 Lines 37-40 of Cutler).

35. In reference to Claim 19, MCF5206, Watanabe, and Beckert, and Cutler disclose the limitations as applied to Claim 18 above. Cutler further teaches that the privileged mode of operation during which the interrupt registers can be accessed is a kernel mode of operation (See Abstract).

36. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the MCF5206, Watanabe, and Beckert as applied to Claim 24 above, and further in view of US Patent Number 5,940,587 to Zimmer ("Zimmer").

37. In reference to Claim 25, MCF5206, Watanabe, and Beckert disclose the limitations as applied to Claim 24 above. MCF5206, Watanabe, and Beckert do not disclose programmable offset storage means, coupled to said vector generator, for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector. Zimmer teaches a programmable offset storage means for providing a programmed offset to a vector generator to allow said vector generator to produce said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of MCF5206, Watanabe, and Beckert with the programmable offset storage means of Zimmer, resulting in the invention of Claim

25, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

38. In reference to Claim 26, MCF5206, Watanabe, Beckert, and Zimmer teach the limitations as applied to Claim 25 above. Zimmer further teaches that the interrupt vector table containing the offset values is created by a system executive, which is equivalent to kernel mode instructions (See Column 3 Lines 30-41).

39. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the MCF5206 and Watanabe as applied to Claim 30 above, and further in view of Zimmer.

40. In reference to Claim 31, MCF5206 and Watanabe disclose the limitations as applied to Claim 30 above. MCF5206 and Watanabe do not disclose examining a programmable offset and calculating an interrupt vector for the one of the interrupts with the highest priority level utilizing said programmable offset. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to calculate said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of MCF5206 and Watanabe with the programmable offset storage means of Zimmer, resulting in the invention of Claim 31, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

41. In reference to Claim 32, MCF5206, Watanabe, and Zimmer disclose the limitations as applied to Claim 31 above. MCF5206 inherently jumps to the interrupt vector in order to access the proper interrupt handler.

Information Disclosure Statement

42. The information disclosure statement (IDS) submitted on 2 June 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

43. The NPL document to Singhal, et al. incorrectly identifies the page numbers. The correct page numbers are 41-49. The Examiner has cited this document with the correct page numbers on the attached Notice of References Cited.

44. The NPL document to Brylow et al. was not listed on the information disclosure statement in accordance with 37 CFR 1.97. The Examiner has cited this document on the attached Notice of References Cited.

Response to Arguments

45. Applicant's arguments filed 30 October 2006 have been fully considered but they are not moot in view of the new grounds of rejection.

46. Applicant has argued that Watanabe teaches nothing concerning interrupts, and MCF5206 only discloses programmable control of non-core generated interrupts (See Page 13). In response, the Examiner notes that, as shown in the above rejections, MCF5206 is being relied upon to teach programmable control of internal peripheral interrupts. However, the internal peripheral interrupts are not core-generated. Watanabe is being relied upon to teach placing peripheral devices, such as those of MCF5206, in the core. When the internal peripherals of MCF5206 are placed in the core, the interrupts generated by those peripherals are core-generated interrupts. Thus, in combination, MCF5206 and Watanabe teach programmable core-generated interrupts.

47. Applicant has argued that there is no motivation to combine MCF5206 and Watanabe, as MCF5206 cannot be modified according to the teachings of Watanabe

(See Pages 14-15). In response, the Examiner notes that Watanabe is not limited to the disclosed components, but may include additional functional blocks (See Column 3 Lines 38-31). Further, the function blocks do not need to have the same size. Watanabe discloses that in cases where some functions blocks have a greater and smaller byte-size than the others, the cells of the bigger blocks in excess of the standard number can be coupled with the smaller blocks to form standard blocks (See Column 3 Lines 32-40). This would, therefore, minimize the area needed for the function blocks by requiring less area for connecting lines (See Column 3 Lines 41-46).

48. In response to applicant's argument that the MCF5206 is more complex than the CPU of Watanabe (See Pages 14-15), the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Because of the complex structure of the MCF5206, one or ordinary skill in the art would naturally look to methods of simplifying the structure, such as that taught by Watanabe.

49. Applicant has argued that the modification of Watanabe would not allow the MCF5206 to be more easily interfaced with various peripheral devices (See Page 15). In response, the Examiner notes that MCF5206 may require a change to the instruction

set to support peripherals other than those disclosed. Watanabe allows various different peripheral devices to be easily incorporated into the system without requiring a change to the instruction set or architecture (See Column 1 Lines 26-38).

50. Applicant has argued that the modification of Watanabe would not minimize the area needed by the MCF5206 microprocessor by reducing the area needed for connecting lines (See Page 15). In response, the Examiner notes that a direct connection to the core would eliminate the need for a bus to interconnect the peripherals and a bus controller to control the bus, thereby reducing the area.

51. Applicant has argued that the modification of Watanabe would not increase the flexibility of program design of the MCF5206, because all of the software operations supported by Watanabe are supported by MCF5206 (See Page 16). I n response the Examiner notes that the flexibility in programming arises from all of the instructions being applicable to all of the accumulators and input/output units in common and all of the addressing modes used to access operands being applicable to all of the input output units (See Column 4 Lines 3-10).

52. Applicant has argued that MCF5206 does not disclose that the priorities of on-core and off-core interrupts are intermediate of one another (See Page 17). In response, the Examiner notes that because there are three external interrupts that are fixed at levels 1, 4, and 7, and five peripheral interrupts programmable to levels 1-7, at

least a portion of the peripheral interrupts must be at levels 2, 3, 5, or 6, and are thus intermediate to the external interrupts programmed at levels 1, 4, and 7.

Conclusion

53. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Section 5 of the Software User's Manual for the MIPS32 Processor Core Family and Section 5 of the Software User's Manual for the MIPS64 Processor Core Family, which were submitted in response to a requirement for information under Rule 105.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJC

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thomas J. Cleary
Patent Examiner
Art Unit 2111